

REMARKS

Claims 1, 2, 4-7 and 9-33 are pending. By this Amendment, claims 6 and 9 are amended.

Entry of the amendments is proper under 37 CFR §1.116 since the amendments are made to clarify the language of the claims.

I. The Claims Contain Allowable Subject Matter

The Office Action rejects claims 6-7 and 9-22 under 35 U.S.C. §103(a) over Fujihara (U.S. Patent No. 5,771,083) in view of Kouchi (U.S. Patent No. 5,886,365), Aoki '916 (U.S. Patent No. 6,177,916) and Sato (U.S. Patent No. 6,081,305) and further in view of Mizuno (U.S. Patent No. 6,266,110), Someya (U.S. Patent No. 5,838,399) and Aoki '857 (U.S. Patent No. 5,425,857); rejects claims 6, 7 and 9-22 under 35 U.S.C. §103(a) over Nakagaki (U.S. Patent No. 6,104,370), in view of Kouchi, Aoki '916 and Sato and further in view of Mizuno, Someya and Aoki '857; rejects claims 6, 7 and 9-22 under 35 U.S.C. §103(a) over Moon (U.S. Patent No. 6,133,967) in view of Kouchi, Aoki '916 and Sato and further in view of Mizuno, Someya and Aoki '857; and rejects claims 6-22 under 35 U.S.C. §103(a) over Kouchi, Aoki '916 or Sato in view of Mizuno, Someya and Aoki '857. The rejections are respectfully traversed.

In particular, neither Fujihara, Nakagaki, Moon, Kouchi, Aoki '916, Sato, Mizuno, Someya nor Aoki '857, individually or in combination, disclose or even suggest a peripheral circuit which is provided with leads comprising a first, second and third conductive layers and drives each switching element, the peripheral circuit having parallel leads in which a lead comprising the first conductive layer and a lead comprising the second conductive layer are electrically connected in parallel with respect to both ends of the parallel leads to reduce wiring resistance, as recited in independent claim 6.

The following explanation is made by way of an example to aid the Examiner in the understanding of claim 6 and should no way be construed as limiting the scope of the claim. The peripheral circuit uses the first, second and third conductive layers. By using the parallel lead in which the lead composed of the first conductive layer and the lead composed of the second conductive layer are electrically connected, the wiring resistance thereof can be reduced compared to the use of the first or second conductive layer alone.

Fujihara discloses an active matrix substrate incorporated in a liquid crystal display device where the storage capacitor line 4 and the oxide insulating films 9 are formed on the light transmitting substrate 1. See, for example, Fig. 3 and col. 6, lines 24-34. Fujihara does not disclose a peripheral circuit. Therefore, Fujihara does not disclose a peripheral circuit having parallel leads in which a lead comprising the first conductive layer and a lead comprising the second conductive layer are electrically connected in parallel with respect to both ends of the parallel leads to reduce wiring resistance.

Nakagaki discloses a silicon substrate 1 including a MOSFET 2 having a drain 5, a gate 6 and a source 7, and a capacitor 3 for storing electric charge corresponding to one pixel. See, for example, Fig. 7 and col. 4, lines 49-60. Nakagaki does not disclose or even suggest a peripheral circuit. Therefore, Nakagaki does not disclose or even suggest the above noted features of the claimed invention.

Moon discloses a liquid crystal display including a thin film transistor (TFT) and a storage capacitor where a gate insulating layer 5 is selectively etched using a gate electrode 3 as a mask. See, for example, Figs. 2A-2E and col. 4, lines 14-30. Moon does not disclose or even suggest a peripheral circuit. Therefore, Moon does not disclose or even suggest the features of the claimed invention.

Kouchi discloses a small size and a large capacitance capacitor is provided for in a peripheral driving circuit of a liquid crystal display device. See Abstract of Kouchi. However,

Kouchi does not disclose or even suggest a peripheral circuit having parallel leads in which a lead comprising the first conductive layer and a lead comprising the second conductive layer are electrically connected in parallel with respect to both ends of the parallel leads to reduce wiring resistance. Therefore, Kouchi does not disclose or even suggest the features of the claimed invention.

Neither Aoki '916, Sato, Mizuno, Someya nor Aoki '857 cure the above noted deficiencies of Fujihara, Moon, Nakagaki or Kouchi.

Aoki '916 discloses in Fig. 1 and in col. 3, line 51 to col. 4, line 10 that the buffer circuits are connected to the analog switches. A timing signal generator circuit provides the buffer circuits with a timing signal. The analog switches supply video signals from the video busses to the signal lines in a display region in response to timing signal. This structure can reduce parasitic capacitance loads so that the bandwidth characteristic of the video busses can be improved and a good display can also be obtained. However, Aoki '916 does not disclose or even suggest the claimed invention.

Sato discloses in Fig. 3 and in col. 15, lines 53-65, that a pixel circuit area 101 is provided in the well region 112 formed in the N-type silicon substrate 111. In the periphery of the pixel circuit area 101, a shading layer 165 formed in the second middle layer 160 is provided, and an electrode 183 which is electrically separated from the electrode 181 is formed in the upmost third middle layer 180 to supply a voltage that is equal to that of an electrode 302 which faces the electrode 183, thereby setting an application voltage of the liquid crystal of the pixel circuit to the periphery to zero. However, Sato does not disclose or even suggest the claimed invention.

Mizuno discloses an upper metal wiring layer is formed of titan Ti and titan nitride TiN formed thereon, on which tungsten W for filling a via hole can be deposited. The via hole is

filled with W. See, for example, Abstract of Mizuno. However, Mizuno does not disclose or even suggest the claimed invention.

Someya discloses a TFT active matrix liquid crystal display devices in which a pixel is divided into three parts, a capacitor is added to each pixel, light shielding is applied to each TFT and the matrix is driven by a DC canceling technique. See, for example, Abstract of Someya. However, Someya does not disclose or even suggest the claimed invention.

Aoki '857 discloses a matrix type display having a TFT substrate where a gate signal line interconnects respective gate electrodes of the TFTs arranged in a row or column of the matrix array, a source electrode line interconnected respective source or drain electrodes of the TFT arranged in a column or row of the matrix array, a pixel electrode formed of a transparent conductor film and connected to the source or drain electrode of each of the TFTs, a capacitor electrode capacitively coupled to the pixel electrode through a dielectric film, a conductor wire interconnecting the respective capacitive electrode of the pixels interconnected by the gate signal line, wherein the conductor wire is formed integrally with the capacitor electrode. See, for example, Abstract of Aoki '857. However, Aoki '857 does not disclose or even suggest the claimed invention.

Because the applied references, individually, of in combination, do not disclose the features of independent claim 6, independent claim 6 defines patentable subject matter. Claims 7 and 9-22 depend from independent claim 6, and therefore also define patentable subject matter. Accordingly, withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

II. Conclusion

In view of the foregoing amendments and remarks, this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1, 2, 4-7 and 9-32 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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